

1 WHAT IS CLAIMED IS:

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3 1. An amplifier comprising at least one output and first and second supply rails,
4 the amplifier further comprising offset cancellation logic which is operable in a calibration
5 mode to generate a first offset cancellation signal when the at least one output is coupled to a
6 first voltage corresponding to the first supply rail, and a second offset cancellation signal
7 when the at least one output is coupled to a second voltage corresponding to the second
8 supply rail, the offset cancellation logic further being operable to facilitate at least partial
9 cancellation of an offset voltage associated with the at least one output during a normal
10 operation mode using a third offset cancellation signal which substantially corresponds to an
11 average of the first and second offset cancellation signals.

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13 2. The amplifier of claim 1 wherein the amplifier comprise one of a switching
14 amplifier topology and a linear amplifier topology.

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16 3. The amplifier of claim 1 wherein the switching amplifier topology employs
17 continuous-time feedback from the at least one output.

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19 4. The amplifier of claim 1 wherein the amplifier comprises one of a single-
20 ended amplifier and a differential amplifier.

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22 5. The amplifier of claim 1 wherein the amplifier comprises multiple channels,
23 each of the channels comprising an instance of the offset cancellation logic.

1 6. The amplifier of claim 1 wherein the offset cancellation logic is operable to
2 generate the third offset cancellation signal during the calibration mode.

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4 7. The amplifier of claim 1 wherein the amplifier comprises a switching
5 differential amplifier, and the at least one output comprises first and second outputs which
6 together form a differential output.

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8 8. The amplifier of claim 7 wherein the offset cancellation logic is operable to
9 generate the first offset cancellation signal when the first and second outputs are coupled to
10 the first voltage, and the second offset cancellation signal when the first and second outputs
11 are coupled to the second voltage.

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13 9. The amplifier of claim 1 wherein the offset cancellation logic comprises a
14 digital-to-analog converter (DAC), a first up/down counter, a second up/down counter, and
15 calibration control logic, the calibration control logic being operable to configure the
16 amplifier for the calibration and normal operation modes, the calibration control logic further
17 being operable during the calibration mode to control the first and second counters and the
18 DAC via one of the counters to generate the first and second offset cancellation signals, the
19 DAC being operable during normal operation mode to generate the third offset cancellation
20 signal.

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22 10. The amplifier of claim 1 wherein the amplifier is optimized for operation in a
23 frequency range.

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1 11. The amplifier of claim 10 wherein the frequency range comprises the audio
2 frequency range.

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4 12. The amplifier of claim 1 further comprising a processor stage and a power
5 output stage, the offset cancellation logic being part of the processor stage.

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7 13. At least one computer-readable medium having data structures stored therein
8 representative of the processor stage of claim 12.

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10 14. The at least one computer-readable medium of claim 13 wherein the data
11 structures comprise a simulatable representation of the processor stage.

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13 15. The at least one computer-readable medium of claim 14 wherein the
14 simulatable representation comprises a netlist.

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16 16. The at least one computer-readable medium of claim 13 wherein the data
17 structures comprise a code description of the processor stage.

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19 17. The at least one computer-readable medium of claim 16 wherein the code
20 description corresponds to a hardware description language.

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22 18. A set of semiconductor processing masks representative of at least a portion
23 of the processor stage of claim 12.

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25 19. An integrated circuit comprising the offset cancellation logic of claim 1.

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2 20. An electronic system comprising the integrated circuit of claim 19.

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4 21. A switching amplifier comprising
5 a power output stage comprising first and second outputs forming a differential
6 output, and first and second supply rails; and
7 a processor stage operable to receive an input signal and generate a processed
8 differential signal for amplification by the power output stage, the processor stage further
9 comprising offset cancellation logic which is operable in a calibration mode to generate a
10 first offset cancellation signal when the first and second outputs are coupled to a first voltage
11 corresponding to the first supply rail, and a second offset cancellation signal when the first
12 and second outputs are coupled to a second voltage corresponding to the second supply rail,
13 the offset cancellation logic further being operable to facilitate at least partial cancellation of
14 an offset voltage associated with the different output during a normal operation mode using a
15 third offset cancellation signal which substantially corresponds to an average of the first and
16 second offset cancellation signals.

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18 22. A method for facilitating at least partial cancellation of an offset voltage
19 associated with first and second outputs of an amplifier, the amplifier having first and second
20 supply rails associated therewith, the method comprising:
21 configuring the amplifier for a calibration mode, and in the calibration mode,
22 setting the first and second outputs to a first voltage associated with
23 the first supply rail;

1 while the first and second outputs are at the first voltage, determining a
2 first offset cancellation signal by which the offset voltage is substantially
3 canceled;

4 setting the first and second outputs to a second voltage associated with
5 the second supply rail; and

6 while the first and second outputs are at the second voltage,
7 determining a second offset cancellation signal by which the offset voltage is
8 substantially canceled; and

9 configuring the amplifier for a normal operation mode, and in the normal operation
10 mode at least partially canceling the output offset voltage using a third offset cancellation
11 signal which substantially corresponds to an average of the first and second offset
12 cancellation signals.

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